WHAT IS CLAIMED IS:

1. An arrangement for suppressing digital-to-analog converter (DAC) error arising from mismatched elements contained in a DAC that is part of a modulator that provides a digital output, the arrangement comprising:

a shifting arrangement configured to controllably shift a digital word derived from the digital output so as to cause a DAC error distribution to constitute a low pass profile suppressing DAC error at higher frequencies around half a sampling frequency.

2. The arrangement of Claim 1, wherein:

the shifting arrangement controllably shifts the digital word using only a single pointer per clock cycle.

3. The arrangement of Claim 2, further comprising:

a low pass averaging (LPA) index decoder that is configured to control the shifting arrangement to shift the digital word in a manner that causes the DAC error distribution to constitute the low pass profile.

4. The arrangement of Claim 3, wherein the LPA index decoder is configured to provide an output according to an expression

$$LPA(j) = LPA(j-1) + \frac{1+(-1)^j}{2} n_Q + \frac{1-(-1)^j}{2} (2^N - n_Q)$$

wherein:

LPA(j) denotes a current pointer value output by the LPA index decoder;

LPA(j-1) denotes a previous pointer value output by the LPA index decoder;

N is a total number of bits in the digital word;

n_Q is a number of logic "1" bits in the digital word; and

j is a clock signal index number.

5. The arrangement of Claim 3, wherein the LPA index decoder includes:

a first plurality of logic gates, each having a first input and a second input, and a first output that is turned on only when a logic 0 is input to the first input and a logic 1 is input to the second input, wherein the first outputs from the first plurality of logic gates collectively control the shifting arrangement at odd numbered clock cycles; and

a second plurality of logic gates, each having a first input and a second input, and a second output that is turned on only when a logic 1 is input to the first input and a logic 0 is input to the second input, wherein the second outputs from the second plurality of logic gates collectively control the shifting arrangement at even numbered clock cycles.

6. The arrangement of Claim 3, further comprising a swapper, configured to receive the digital output and to provide to the shifting arrangement, on alternating clock cycles, respectively:

i) the digital output; and

ii) a swapped output containing bits of the digital output in reverse order.

7. The arrangement of Claim 3, wherein:

the digital output, the digital word input to the shifting arrangement and an output of the shifting arrangement, are all thermometer codes.

8. The arrangement of Claim 1, further comprising:

a low pass averaging (LPA) index decoder that is configured to control the shifting arrangement to shift the digital word in a manner that causes the DAC error distribution to constitute the low pass profile.

9. The arrangement of Claim 8, wherein the LPA index decoder is configured to provide an output according to an expression:

$$LPA(j) = LPA(j-1) + \frac{1+(-1)^j}{2} n_Q + \frac{1-(-1)^j}{2}(2^N - n_Q)$$

wherein:

LPA(j) denotes a current pointer value output by the LPA index decoder;

LPA(j-1) denotes a previous pointer value output by the LPA index decoder;

N is a total number of bits in the digital word;

n_Q is a number of logic "1" bits in the digital word; and

j is a clock signal index number.

10. The arrangement of Claim 8, wherein the LPA index decoder includes:

a first plurality of logic gates, each having a first input and a second input, and a first output that is turned on only when a logic 0 is input to the first input and a logic 1 is input to the second input, wherein the first outputs from the first plurality of logic gates collectively control the shifting arrangement at odd numbered clock cycles; and

a second plurality of logic gates, each having a first input and a second input, and a second output that is turned on only when a logic 1 is input to the first input and a logic 0 is input to the second input, wherein the second outputs from the second plurality of logic gates collectively control the shifting arrangement at even numbered clock cycles.

11. The arrangement of Claim 8, further comprising a swapper, configured to receive the digital output and to provide to the shifting arrangement, on alternating clock cycles, respectively:

i) the digital output; and

ii) a swapped output containing bits of the digital output in reverse order.

12. The arrangement of Claim 8, wherein:

the digital output, the digital word input to the shifting arrangement and an output of the shifting arrangement, are all thermometer codes.

13. A shifting arrangement, comprising:

a shifter configured to shift a digital input word in a first direction on even-numbered clock cycles and in a second direction opposite the first direction on odd-numbered clock cycles that alternate with the even-numbered clock cycles, and to provide a resulting shifted digital word that constitutes the digital input word shifted by a number of bit positions determined by a shift control word; and

a decoder, configured to calculate, based at least in part on the shifted digital word, the shift control word that determines a number of bits by which the shifter shifts the digital input word to form the resulting shifted digital word.

14 The shifting arrangement of Claim 13, wherein:

the shifter is a barrel shifter.

15. The shifting arrangement of Claim 13, wherein:

the decoder provides a single pointer per clock cycle to the shifter.

16. The shifting arrangement of Claim 13, wherein:

the shifter is contained in a modulator that includes a digital-to-analog converter (DAC) having mismatched elements causing errors that are characterized by a DAC error distribution; and

the decoder constitutes a low pass averaging (LPA) index decoder that is configured to control the shifter to shift the digital word in a manner that causes the DAC

error distribution to constitute a low pass profile suppressing DAC error at higher frequencies around half a sampling frequency.

17. The shifting arrangement of Claim 16, wherein the LPA index decoder is configured to provide an output according to an expression:

$$LPA(j) = LPA(j-1) + \frac{1+(-1)^j}{2} n_Q + \frac{1-(-1)^j}{2}(2^N - n_Q)$$

wherein:

LPA(j) denotes a current pointer value output by the LPA index decoder;

LPA(j-1) denotes a previous pointer value output by the LPA index decoder;

N is a total number of bits in the digital input word;

n_Q is a number of logic "1" bits in the digital input word; and

j is a clock signal index number.

18. The shifting arrangement of Claim 16, wherein the LPA index decoder includes:

a first plurality of logic gates, each having a first input and a second input, and a first output that is turned on only when a logic 0 is input to the first input and a logic 1 is input to the second input, wherein the first outputs from the first plurality of logic gates collectively control the shifter at odd numbered clock cycles; and

a second plurality of logic gates, each having a first input and a second input, and a second output that is turned on only when a logic 1 is input to the first input and a logic

0 is input to the second input, wherein the second outputs from the second plurality of logic gates collectively control the shifter at even numbered clock cycles.

19. The shifting arrangement of Claim 16, further comprising a swapper, configured to receive a digital output of the modulator, and to provide to the shifter, on alternating clock cycles, respectively:

the digital output; and

a swapped output containing bits of the digital output in reverse order.

20. The shifting arrangement of Claim 16, wherein:

a digital output of the modulator, the digital input word input to the shifter and resulting shifted digital word output by the shifter, are all thermometer codes.

21. A method for suppressing digital-to-analog converter (DAC) error arising from mismatched elements contained in a DAC that is part of a modulator that provides a digital output, the method comprising:

controllably shifting a digital word derived from the digital output so as to cause a DAC error distribution to constitute a low pass profile suppressing DAC error at higher frequencies around half a sampling frequency.

22. The method of Claim 21, wherein the shifting step includes:

shifting the digital word using only a single pointer per clock cycle.

23. The arrangement of Claim 22, further comprising:

using a low pass averaging (LPA) index decoder to cause the digital word to be shifted in a manner that causes the DAC error distribution to constitute the low pass profile.